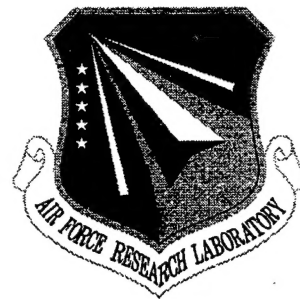


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ADMISSION CONTROL AND ROUTING ALGORITHMS FOR ATM NETWORKS

Washington State University

Cauligi S. Raghavendra

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APPROVED: 
BRADLEY J. HARNISH
Project Engineer

FOR THE DIRECTOR: 
WARREN H. DEBANY, JR., Technical Advisor
Command, Control & Communications Directorate

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Admission Control and Routing Algorithms for ATM Networks

1 Executive Summary

In this research project, several issues related to providing Quality of Service (QoS) for command and control applications running on ATM networks were investigated. The QoS requirements are specified in terms of maximum delays, jitter, and cell loss probability. In this context, new ATM switch designs, algorithms for traffic control, routing and multicasting were developed. Novel neural network based techniques for traffic characterization, admission control at node and network level were developed. A new multicast switch architecture was designed for use in high performance ATM network and its performance evaluated via simulation. New Algorithms for efficiently routing ATM cells in input buffered switches were developed and their performance evaluated. Algorithms for routing multicast traffic in wide area ATM network were developed for use in ATM Forum's Private Network to Network Interface (PNNI) hierarchy. These algorithms were designed to handle QoS requirements. The admission control and routing algorithms are evaluated through extensive simulations. Many of the techniques and algorithms developed in this research project are also applicable to high-speed Internet.

2 Introduction and Overview of the Project

The emerging Broadband Integrated Services Digital Network (B-ISDN) will support multimedia services, including voice, video and data communications. Asynchronous Transfer Mode (ATM) is the standard for implementing B-ISDN, and is designed to provide communications services over a wide range of bit rates. ATM is a high-speed packet switched network, in which all information is segmented into a series of short fixed-size packets called cells. The ATM network has extensive flexibility and a wide variety of arbitrary bit-rate communication media which can be combined into one service by cell multiplexing.

ATM networks are predicted to play an important role in the future because of their capacity to handle high bandwidth and their ability to support Quality-of-Service(QoS) guarantees. This support is the basis for the development of multimedia applications. ATM networks consist of ATM switches (also known as nodes) interconnected by point-to-point links. The data in ATM networks is transmitted in the form of fixed length packets called *cells*. The standards specify the fixed length as 53 bytes, which includes a 5-byte header. The header contains information that is used to route the data cells from the source to the destination. The segmentation of data into 48-byte chunks at the source and the reassembly of data at the receiver is performed at a higher layer called the ATM Adaptation Layer(AAL). At present, AAL5 is the specified standard for data applications.

The ATM networks are fundamentally connection-oriented, i.e., a virtual connection has to be established between two end-points before data can be transferred across the network. The virtual connection is identified by the combination of a Virtual Path Identifier(VPI) and a Virtual Channel Identifier(VCI). The actual values of the VPI/VCI have only a local significance on a given link. These values are a part of the ATM cell header. Therefore, when the ATM cells are switched from one link to another at a switch, the VPI/VCI values are also translated. Since the VPI/VCI fields are small and of fixed length, the switching of ATM cells can be performed by hardware. Therefore, the hardware intensive ATM switches are capable of high-speed switching and handling very high bandwidth.

In an ATM network, cells belonging to a connection can possibly go through several switches. At each switch, cells of a connection is routed to the desired output by the switches using the VCI information. For traffic switching, many types of switching fabrics have been proposed for use in ATM networks. These include crossbar switches, input buffered switch, output buffered shared memory switch, and multi-stage switching fabrics. Larger switches are built using smaller switching elements. ATM switches play a critical role in routing cells to their correct destinations. They

also make important decisions like bandwidth allocation for a connection and admission control. ATM networks support connection oriented service with Quality of Service (QoS) for connections. All cells belonging to a connection must be delivered in the same order it is generated at the source.

The main research issues and problems focused in this research project were admission control and routing algorithms for ATM networks. The solutions to these problems play an important role in providing QoS for applications running over ATM networks. QoS measures such as bounded maximum delays, jitter, and cell loss probability are critical to command and control applications. Traffic control in ATM networks can be achieved through admission control and bandwidth allocation and enforcement. Admission control decides, based on traffic characteristics, whether to accept a new connection at call set up time. In an ATM network, many low-speed traffic streams are multiplexed onto a high-speed link. This is achieved by statistical multiplexing of the input streams into one outgoing stream and admission control is essential to control the total input traffic to meet QoS requirements. In this research, we investigated and developed new algorithms based on neural networks for admission control at an ATM multiplexer as well as in an ATM network consisting of multiple nodes.

An important design objective of ATM networks is to provide integrated services for different types of traffic, namely, voice, video, and data. Different types of traffic have different characteristics and QoS requirements. For example, video traffic can handle more cell loss than audio traffic. When these types of traffic is combined at an ATM multiplexer, it can modify some of the traffic characteristics from the input stream to output. We have studied such effect on jitter at a multiplexer when an audio stream is combined with several video streams. Also, if we can predict the future traffic, we can allocate buffers suitably to achieve improved traffic characteristics (shape the traffic) for succeeding switches. We have used neural networks to predict video traffic and such a technique is viable for predicting a few frames ahead based on the previous set of frames in video traffic.

The other area of focus for this project was on routing algorithms. In this area we developed new algorithms for routing traffic through ATM switches, designed a switch that supports multicast traffic routing, and developed efficient algorithms for multicast routing in ATM networks under the ATM Forum's Private Network to Network Interface protocol framework. The techniques developed are applicable to other high-speed networks and the details of the algorithms and results are explained later in this report.

The following are the major accomplishments of this project:

- **Connection Admission Control:** Novel admission control schemes were developed to support QoS at node level and network level. The techniques used were based on neural networks and the performance is evaluated via simulation.
- **Jitter Characterization:** The effect of mixing a periodic source with other traffic is analyzed to determine the statistical characterization of jitter at an ATM multiplexer. This analysis of jitter helps in traffic shaping and for providing quality of service for connections.
- **Design of a Multicast ATM Switch:** Designed an ATM switch fabric based on expanded tandem delta networks that achieved better throughput for multicast traffic than other existing switching fabrics.
- **Routing Algorithms:** Schemes were developed for routing cells in input buffered switches. The technique used is based on bipartite graph matching followed by permutation routing so it can be used in low cost Benes switching networks.
- **Multicast Routing in ATM Networks:** Developed hierarchical, scalable, and distributed multicast routing protocols for use in large ATM networks.

Our objectives and goals were to design new methodologies for admission control, study traffic characteristics, and develop routing and multicasting algorithms. These objectives were met in our investigations during the past three years and we have identified several new and interesting problems in this area. The details of the research findings are summarized in the following sections. The research results have appeared in many publications and some more are being prepared for future publications.

3 Connection Admission Control

Network resources have to be fairly allocated to the various traffic types in ATM networks. Admission control is one of the congestion control mechanisms executed at virtual call setup time. The primary function of the connection admission control is to accept a new connection only if its QoS requirements can be met without affecting the performance of existing connections. The admission control protocol must decide whether connections can be accepted or not, provide traffic parameters to accurately predict network performance, and perform routing and resource allocation. Admission control algorithms use general traffic characteristics of input traffic and its performance depends on the accuracy of these traffic parameters. A set of

traffic descriptors, such as peak rate, average rate, and a measure of burstiness are commonly used parameters. Characterizing the burstiness of a traffic is a difficult issue: several types of descriptors have been used in various traffic control schemes. The ratio of peak to average bit rate is used in [12, 14]. The burst length seems to be an important factor as it significantly affects the performance [14].

Traditional control methods based on thorough analysis of offered traffic descriptors cannot achieve high performance. This is due to the fact that it is difficult to optimize the number of connections that can be admitted without affecting QoS for existing connections because of statistical multiplexing of sources and variations in input traffic. The problem is simpler for constant bit rate traffic. The control algorithm must balance the QoS requirements while maximizing the utilization. Neural networks are useful for solving this type of optimization problems as they can produce good results with incomplete information [13, 16, 17, 1]. Neural networks have the ability to learn traffic features from past history of inputs to make good decisions. There are many types of neural networks and after studying various approaches, Fuzzy-ARTMAP was chosen for design of our new admission control algorithms.

We developed an approach to the admission control problem using the Fuzzy-ARTMAP network and Backpropagation network. From our experiments we found that the admission control can be effectively accomplished using the Fuzzy-ARTMAP neural net. Fuzzy-ARTMAP meets the speed restrictions and does not pose the problem of parameter crafting and of temporal instability. Backpropagation is a good generalizer and can be used for admission control though speed and possible temporal instabilities are some concerns. The algorithm based on Fuzzy-ARTMAP is fast, requires no fine tuning of parameters and does not suffer from temporal instability during on-line training which could be a problem with the Backpropagation neural network. The QoS parameter considered is cell loss in video traffic and cell arrival information was used from real video data sources for the simulation.

The admission control algorithm uses the cell loss as the QoS parameter in making decisions, where cell loss is defined as the ratio of cells dropped to the link capacity. Each incoming connection request sends the peak bit rate and average bit rate traffic descriptor. The controller, being the neural network, places this incoming connection in accept/reject based on its prediction of cell loss. The neural controller would be initially trained with a large set of traffic pattern to make it robust. Then as new connections come in, the neural net is trained with this new pattern by adding this connection and dropping one from the training set. We did extensive simulations using various call combinations to determine the efficiency of the controller. We were mixing various video traffic streams with different rates and simulated multiplexing traffic

onto a 155 Mbps link. Both Backpropagation neural network and Fuzzy-ARTMP were tested for this decision problem. Our results show that the Fuzzy-ARTMAP controller performed well when several different traffic types are mixed.

It is important to retrain the network periodically so that the learning takes place dynamically to yield good identification. To facilitate such on-line training we used a window scheme, where each window has a set of call combinations. Essentially, each window represents an area of the state space. When we add and delete pattern, only one particular window is affected and the network as a whole is trained on the entire state space. Fuzzy-ARTMAP requires fewer examples to train and it has the ability of not forgetting the pattern it has already learnt. Hence, it is fast, requires no fine tuning of parameters, and has no temporal instability. Details of the on-line training scheme and further discussions on the simulation results are given in [19].

4 Jitter Characterization

In ATM networks, significant gains in connection admissions are achieved due to statistical multiplexing of various traffic. Variable rate traffic may generate bursty traffic, and hence, we can allow more than the total peak rate traffic into a multiplexer as on the average we can still maintain acceptable delays for traffic. When constant bit rate or periodic traffic is combined with variable rate traffic at a multiplexer, the traffic characteristics of the periodic source can be quite different from the input side. This is measured by the jitter which is related to the variance in delays for different cells. For certain sessions, this jitter should be bounded.

Jitter for periodic traffic is defined as the distortion of the periodic nature of the cell arrival process at the multiplexing stages of the network. We developed an analytical model using queuing theory to determine the statistical properties of the jitter in a periodic source when it is mixed with bursty traffic at a multiplexer. In our analysis, we considered two types of traffic entering a queue at the multiplexer – cells belonging to periodic class and cells belonging to ON-OFF source class. With our model, we derived queue length distribution immediately before a cell arrival from periodic source. This variations in queue length prior to arrival of periodic cells directly affects the jitter for the periodic source. We also derived the steady state queue length and derived the statistical distribution of jitter.

We observed that the jitter is very sensitive to the number of ON-OFF sources in addition to the variability of each source. Our analysis showed that the cells leaving a multiplexer has a traffic distribution that can be quite different from the original distribution. We also found that the traffic distortion is not limited to periodic

sources. In fact, the departure distribution of any arbitrary renewal arrival process bears little resemblance to the original arrival distribution. It is clear that while statistical multiplexing enables efficient and cost-effective transport, jitter control at the intermediate switching points is necessary for guaranteeing the QoS requirements of real-time traffic. Detailed discussion on the queuing models and the results on the jitter characterization can be found in [35].

5 Multicast Switch Design

The goal of ATM networks is to support integrated media and a wide variety of services with high performance. Many applications require multicast connections, therefore, it is important for ATM switch architecture to support multicast routing function in addition to unicast routing. Several switches have been designed and additional functions have been added in switching elements to support multicasting [24, 41, 9]. High speed networking applications like video-on-demand require the support of switches which can handle very high multicast loads. These switches must be fast and the routing delays for the packets must be small. The switches studied in the literature can support multicast loads (ratio of number of multicast packets to total number of packets) of 25-30% without much degradation in performance. But, for higher loads, the delays of the packets can be very large. We designed a new ATM switch which can withstand multicast loads of 85-90% without a loss in performance. The switch has very low latency, small packet routing delay and minimal buffering. These features make the switch an attractive component for future high-speed networks.

Many different switch architectures based on multi-stage networks have been proposed to support multicast [24, 5]. One of the earliest design was by Turner [41]. The basic idea in these switches is to use first part of the network to make the desired number of copies of cells and then in the second part of the network route the cells to the correct destinations. For example, in Lee's design[24] a *Copy Network* is used to make copies of the multicast packets, one for each output destination, and then a *Routing Network* is used to route these packets to the desired destination. This switch design still has output contention, and therefore, packets cannot be routed in a cycle need to be buffered at the inputs and they contend with new arrivals in the next cycle.

The output contention exists in most designs due to the fact that only one packet can be delivered to an output in a cycle. To alleviate this problem, an enhanced switch based on the Expanded Delta Network(EDN)[3] has been developed. An $N \times N$ EDN

switch, with an expansion factor of K , has K interleaved $N \times N$ delta networks. If $M = K * N$, the EDN can be considered as $M \times M$ delta network with $\log N$ stages. But, only N out of the M inputs have packets. An output line m corresponds to the output address $(m \bmod N)$. Thus, there are K output lines for a given output address. This fact is exploited in reducing the output contention. Since output contention is magnified while multicasting, any reduction in output contention is crucial to the design of multicast switches.

Another approach to improving the throughput is by preventing packets of a particular cycle contending with packets of the next cycle, Tobagi *et al* use a series of Banyan networks to create Tandem Banyan Switch Fabric(TBSF)[39]. Packets which cannot be routed correctly by a Banyan network are marked as “mis-routed” and they are then passed on to the next Banyan network. Since these packets are not fed back to the original network, they do not contend with the packets of the subsequent cycle. Moreover, the number of packets to every subsequent Banyan network decreases, thus, decreasing the chances of contention. The drawback of this design is that a large number of Banyan blocks have to be connected in tandem to achieve acceptable packet loss ratios and this increases the latency of the packets. Secondly, the authors did not use their network for multicasting, which would have further increased the number of Banyan blocks required for acceptable packet losses.

Our design uses an augmented Expanded Delta Network and connects several of them in tandem. Thus, our design combines the advantages of expanded delta networks and the tandem Banyan networks. Also, the combined features overcome the disadvantages present in the individual designs. For example, in EDN, the packets which cannot be routed are buffered in the input stage, where they compete with the packets which arrive in the subsequent cycle. In our design, packets are buffered at the input only if the total number of copies for all the input packets at a given clock cycle exceeds the total number of output lines. Even for heavy multicast loads, the buffering is infrequent. No buffering is required for the routing network because of the tandem blocks of the network. The TBSF has a large latency. But the enhanced network structure of EDN reduces the number of collisions within the routing network, thus keeping the latency within reasonable values. More details of the switch and its performance results for multicast traffic can be found in [42].

6 A Cell Routing Algorithm for Input-Buffered Switch

In an ATM network, cells belonging to a connection can possibly go through several switches. At each switch, cells of a connection is routed to the desired output by the switches using the VCI information. There is a wide variety of switching fabrics proposed for ATM traffic switching. These fabrics can be broadly classified into tree types – input-buffered switches, output-buffered switches, and shared memory switches. Typically, ATM switches are designed for N inputs and N outputs, where N ranges from 8 to 64. Larger switches are built using smaller switching elements.

ATM networks support connection oriented service with Quality of Service (QoS) for connections. All cells belonging to a connection must be delivered in the same order it is generated at the source. The goal in switch routing is to achieve high throughput with certain QoS requirements satisfied. An important issue for routing in switching fabrics is blocking or contention, which occurs when two or more paths needs to go through the same resource. There can be output contention or network blocking. In switching networks, such as the crossbar or the Benes networks, there is only output contention.

Our interest is in efficient routing of cells in input-buffered switches. The simplest non-blocking input-buffered switch is the crossbar switch. In an $N \times N$ crossbar switch, cells arriving at each input is queued at the respective input-buffers. The queues can be served by the switch in sending cells from an input to the desired output. However, in each cycle, an output can only receive one input cell. Output link contention will result when multiple inputs have cells for the same output. If the input queues are served in FIFO order, then among all the Head-of-Line (HOL) cells, we can choose those cells that are going to distinct outputs. However, it is shown in [22] that a crossbar serving HOL cells only can achieve a maximum throughput of about 58%.

In output-buffered switches cells will queue up at the outputs into N separate queues, one for each output. In a cycle the switch can deliver one cell from each of these queues to the output links. It has been shown that this approach can achieve high throughput and has been implemented in several ATM switches with the output queues implemented in shared memory. Although output queuing can achieve high throughput, there are some drawbacks. Since cells from inputs going to the same output get queued in one queue, cell loss could occur if there is no room in the buffer due to bursty arrival of cells to that output. This is alleviated to some extent by using shared buffer memory rather than partitioning the memory among the queues.

Another drawback is providing fairness to the users. Since the output queues are served FIFO it is possible for some inputs to experience long delays due to bursty arrivals at other inputs. Further, output queueing switches require fast memory as in each cycle N reads and N writes need to be completed, which limits the speed of operation.

For these reasons and to design very high-speed switches, there is significant interest in using input-buffered switches in ATM networks [2, 23, 38, 27]. In order to increase the throughput of input-buffered switches, one can avoid the HOL blocking by searching for cells in each input buffer to avoid output conflicts, thereby increasing the number of cells that can be routed in each cycle. Note that the ordering can still be maintained for cells belonging to the same VCI. It has been shown, theoretically, that arbitrarily close to 100% throughput can be achieved with input-buffered switch if we search all the cells in input buffers. One can also maintain separate queues for cells going to different outputs at each input link, and then we only need to select from HOL cells of these N sub-queues for all the input links. Therefore, we may be searching a total of at most N^2 cells to select a possible maximum of N cells to route in a cycle. The procedure for searching in input buffers must be very efficient as the time for each cycle is small.

This problem of searching for cells in input buffers to maximize the number of cells that can be routed in a cycle can be modeled as a bipartite graph matching problem. With the possibility of N cells from each input link, this bipartite matching will have to be done in a graph with $O(N)$ nodes and $O(N^2)$ edges. However, for successive cycles, we will be adding only at most N edges and resolving the bipartite graph matching problem. This maximal matching in a bipartite graph can be solved using a network flow algorithm in $O(N^3)$ time. Several researchers have used randomized algorithm for this searching problem. It is shown in [2] that by using $\log N$ iterations it is possible to achieve maximal matching with high probability. The advantage of randomized algorithms is that it is very simple to implement and gives very good results on the average. These randomized schemes are looking at least N -deep in each input buffer, i.e., selecting N cells from each input, in selecting maximum number of cells to route through the switch in a cycle.

6.1 Routing in Low Cost Benes Network

Recently, a low-cost non-blocking switch, the Benes network, with input buffers is proposed as a possible candidate for high-performance ATM switch [26]. The Benes network being a rearrangeable network, again, we can always route a given set of from inputs to distinct outputs. Thus, the problem of searching the input buffers

for cells going to distinct outputs can be solved by modeling it as a bipartite graph matching problem. The authors in [26] use a sequential search procedure by looking in each input buffer to a depth varying from $N/2$ to $5N/2$ and show that 95% or better throughput can be achieved in switches of size up to $N = 64$. Their searching considers both output contention and network link contention. Clearly, the complexity of this search procedure is $O(N^2)$ and there is no guarantee of obtaining maximal match in each cycle with this sequential search.

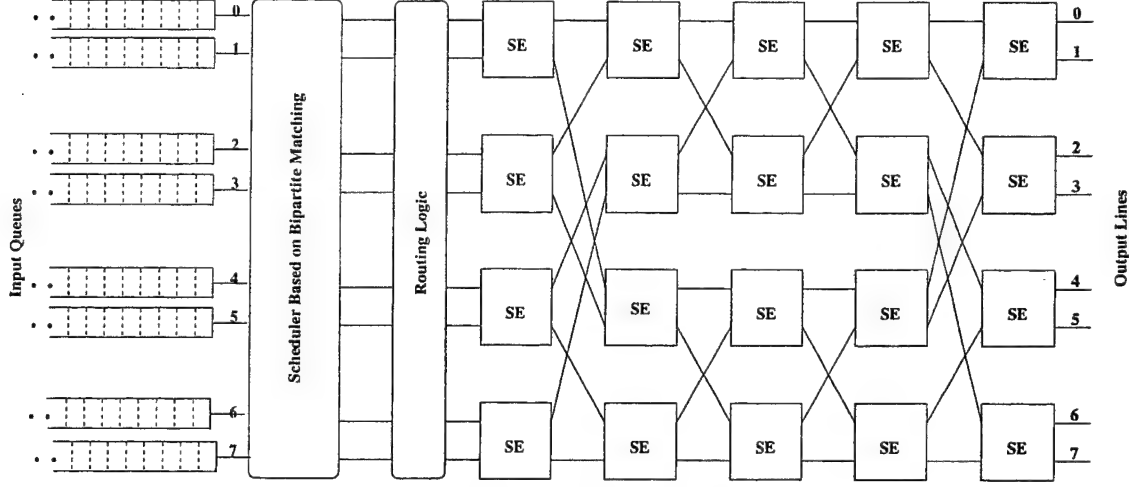


Figure 1: Benes Network as an ATM Switch

In this research project, we developed new algorithms for scheduling traffic in an input-buffered Benes network. This network is rearrangeably non-blocking, i.e., it can route any arbitrary permutation. Therefore, we only need to resolve the output conflicts in selecting the cells to be routed in a step. Our approach was to maintain a single queue at each input link and search for cells deeper in these queues to avoid HOL blocking. The randomized scheme used in the digital switch [2] achieves high throughput by searching in N^2 queues (N sub-queues at each input) and performing maximal match. Our idea was that we should be able to achieve high throughput with limited search in each input queue (examine only small number of cells in each queue) and select the maximum number of cells without output contention for routing.

This routing problem is solved in two phases – bipartite graph matching and routing in the Benes network. The ATM switch fabric for $N = 8$ is shown in Figure 1. In the Benes network, we can always route a given set of inputs that are going to distinct outputs. This is routing a partial permutation (unassigned inputs can go to random unassigned outputs) and efficient algorithms exist for routing such partial permutations in $O(N \log N)$ sequential time [31] and $O(\log^2 N)$ parallel time [25]. To reduce the time for selecting input cells for routing, we will only look k deep into each

input buffer, for small constant k . Therefore, our bipartite graph will have $2N$ nodes and at most kN edges. We used the efficient Dinic's algorithm for network flow with unit weights to solve the bipartite graph matching problem. The time complexity for selecting input cells for routing in this case is, therefore, $O(N\sqrt{N})$. The value for k ranges from 5 to 7 for switch sizes up to $N = 64$. For this practical switch size the complexity of our algorithm is more like $O(N \log N)$. So, essentially, we obtain exact or maximum matching to select input cells by looking only for a small number of cells in each input buffer. Our simulation results show that with this approach we can obtain throughput greater than 95% and is significantly better than using randomized algorithms with $\log N$ iterations as well as the sequential method of [26].

To compare the performance of our algorithm with previously published works, we evaluated our scheme through extensive simulations. In our simulations, we used 100% input load and computed the throughput achievable with different switch sizes and values of the parameter k , the number of cells looked in each input buffer. We also computed throughput under the same conditions for matching with randomized algorithm [2] and for the scheme given in [26]. For the iterative randomized matching, we used exactly $\log N$ iterations of matching. Figure 2 shows our simulation results for switch sizes ranging from 8 to 64. Our results show that using the maximum matching algorithm, we need to look far less number of cells in each input queue compared to the randomized scheme and the method of [26]. It is sufficient to look only about 7 cells in each input queue to achieve a throughput of more than 95%.

7 Multicast Routing

The ATM Forum has standardized the routing and signaling protocols for establishing point-to-point connections in ATM networks. Routing involves the mechanisms used for the computation of the path to be used for the connection. Signaling involves the actual establishment, maintenance and tearing down of the connection. In order to compute efficient paths, the routing protocol provides mechanisms for gathering and maintaining the topology information. The topology information of a network comprises of the state information pertaining to the links and the nodes of that network. This state information includes parameters like the delay across a link (or node), the available bandwidth of a link (or node) and the reliability of the link (or node). This information is pertinent to the computation of an efficient route across the network. Efficient routes result in better utilization of the network resources. The routing and signaling protocols have been designed to be highly scalable to very large networks. This is achieved by providing a hierarchical framework for the ATM

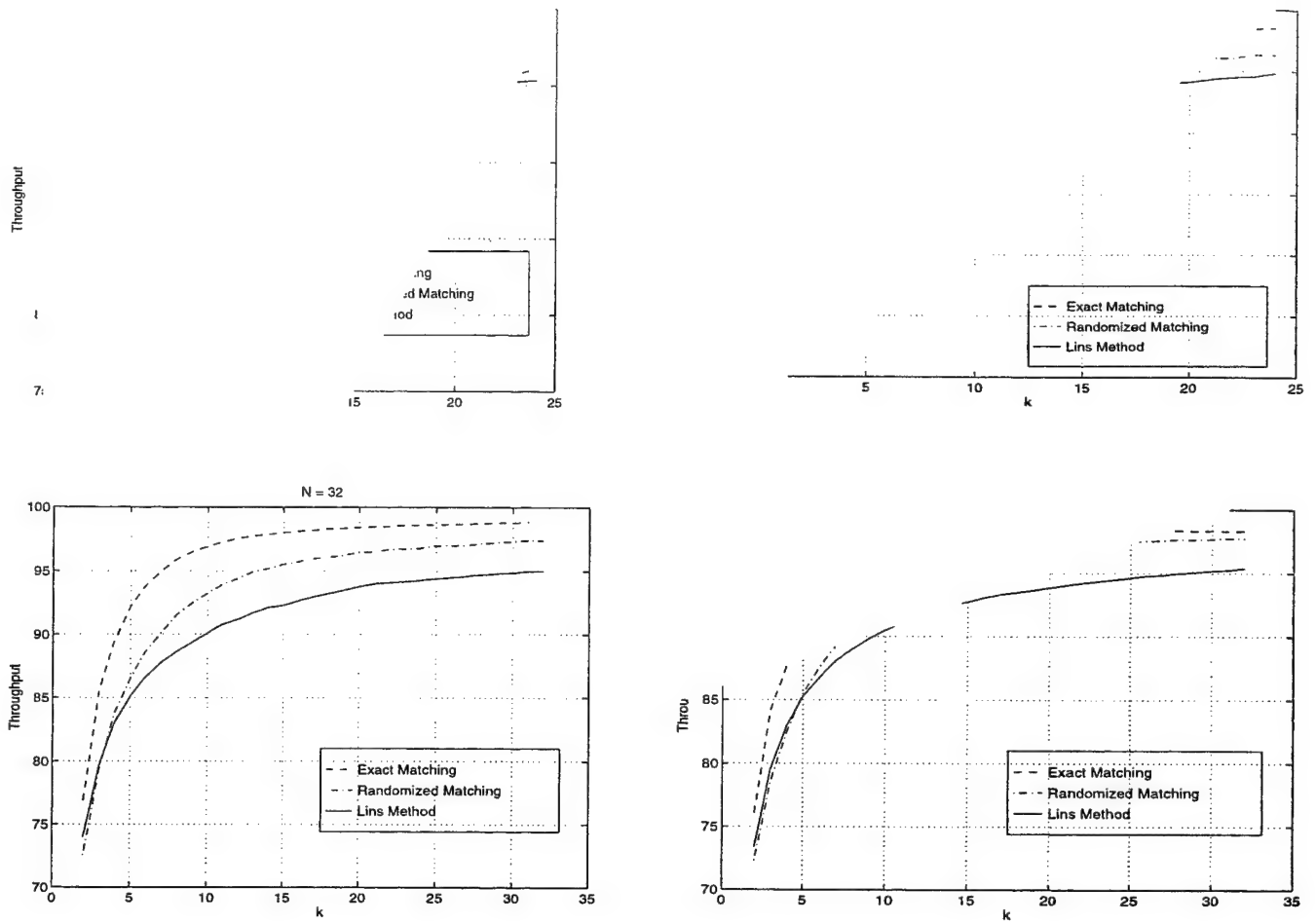


Figure 2: k vs. Maximum Throughput

network. This framework is the basis for the Private Network-Network Interface (PNNI) protocols [33]. The current specification provides excellent support for point-to-point connections. But, at present, support for multicast applications in ATM networks is rudimentary.

Multicasting involves sending data from a sender to multiple receivers simultaneously using a single connection. The multicasting support can be provided at any of the seven OSI layers. If the network layer cannot support such a connection method, the data can still be sent to multiple receivers using a separate point-to-point connection from the sender to each of the receivers. The application then has to manage the set up and maintenance of the multicast session. This feature is evident in the Internet in the form of applications like E-mail (e.g, mailing lists), Usenet news and updating of mirrored FTP sites. Such a mechanism, albeit inefficient and slow, may be sufficient *only* for the applications mentioned above.

Future multimedia applications like video-servers, interactive video-games and

distributed interactive simulations which are likely to scale to large networks, require more efficient and fast multicast support. It is, therefore, desirable that multicast support be provided at the lower layers because this relieves the higher layers from the responsibility of managing these connections. The underlying network has to provide multicast support to efficiently manage existing services as well as future applications.

In this research project, our objective was to design an efficient scheme for multicasting in ATM networks. A study of the protocols designed for multicasting in datagram networks shows that these protocols are not very efficient for ATM networks. The main reason is that these protocols have been designed specifically for datagram networks. Therefore, they support "soft-states" for managing the multicast connection. In other words, the multicast connection is periodically refreshed by the data packets. The periodic refresh makes it easy to periodically recompute the multicast tree to adapt to changes in network states and multicast group membership. The data packets themselves are used to construct the multicast tree. Moreover, the protocols are designed for symmetric links, that is, links that have identical state parameters in both the directions.

ATM networks are connection-oriented networks and therefore, it is not easy to periodically recompute the multicast tree. It makes sense to compute efficient multicast trees before the connection is established. Moreover, it must be remembered that the links are unidirectional and may have different capacities in each direction. This has to be factored into the protocol used to compute the multicast tree. Signaling mechanisms are used in ATM networks to establish the multicast connection. Therefore, efficient multicast trees can be computed during this connection establishment phase. The data cells are then transmitted along the links of the established multicast tree.

Our research focused on providing efficient multicast support for ATM networks. Support for multicasting favors sharing of resources and ease of connection management. The sharing of resources is required for better utilization of resources. Our hierarchical multicast protocol computes a single, shared multicast tree to be associated with a multicast connection. All the participants (senders and receivers) are attached to this tree. The links of this tree are used to send the multicast data from the respective senders to all the receivers.

It has been shown that the computation of multicast tree can be reduced to the well-known Minimal Steiner Tree(MST) problem in graphs. The MST problem is known to be NP-Complete. Therefore, a polynomial-time algorithm to solve the problem is unlikely to exist. But, there are several polynomial-time heuristics which

compute near-minimal Steiner Trees. The worst-case bound for the solutions computed by these heuristics is a factor of 2. For most heuristics, the average-case bound is close to unity.

To support dynamically changing multicast groups, it is necessary that the multicast tree is minimally disturbed after each change in group membership. Recomputing the multicast tree after each change can be computationally expensive. Moreover, it may affect the connection states of existing participants that may cause the data cells to arrive out of sequence. This is against the philosophy of connection-oriented networks like ATM. Therefore, the heuristics designed for the dynamic Steiner Tree problem are used to compute the multicast tree.

Computation of efficient multicast trees is possible only if the topology information and the multicast group membership information is available to all the nodes. The hierarchical framework used to improve the scalability necessitates the maintenance of only partial topological information at each node. Lack of complete topological information complicates the computation of the multicast tree. We solve this problem by proposing extensions to the dynamic Steiner Tree heuristics so that it works under a hierarchical framework. Based on extensive simulations, we show that our heuristics produces solutions that are close to the optimal solution. We also developed the associated routing and signaling protocols to support multicast connections in ATM networks. One of the protocols developed in this research is a hierarchical extension of the Core-Based Tree (CBT) protocol proposed for IP Multicasting. The extension involves selection of multiple core nodes and hierarchically executing a version of CBT modified to work for connection-oriented networks. We show using simulations that this protocol computes efficient multicast trees in most cases. We also propose several schemes for selecting a good set of core nodes. Based on experimental evaluations, we identify the various factors that affect the process of core node selection.

We also developed a flooding approach and a distributed approach to compute efficient multicast trees in a hierarchical framework. In the flooding approach, the multicast group membership information is flooded to all the nodes. On the other hand, in the distributed approach, the membership information is computed using a distributed protocol at the time of connection establishment. The associated routing and signaling protocols necessary to establish the multicast connections were also proposed for the two approaches. We analyzed these protocols and showed that they function correctly and compute efficient multicast trees with minimal overheads. The analysis is verified using extensive simulations.

All the protocols developed by us in this research support Participant-Initiated Joins (PIJ). The protocols are fully compatible with the existing PNNI routing and

signaling protocols. This is required for the scalability of the multicast support mechanisms to large networks, large groups and frequent changes to membership. In addition, low maintenance overheads and simplicity of implementation are the characteristic features of our protocols.

In this research project we have designed new protocols for multicast support in ATM wide area networks under the PNNI framework. We have developed a hierarchical multicast protocol which is based on finding a near optimal Steiner tree dynamically. We also extended this protocol to a distributed version including handling of dynamic memberships. These protocols use leaf initiated join approach and produce efficient trees for multicast communication in PNNI hierarchy. This approach also help in building trees that support QoS requirements. More details on our multicast protocols can be found in [43, 44].

8 Conclusions and Future Work

In this research project, several important problems in high speed networks were investigated. Specific problems studied include admission control protocols, cell routing algorithms, traffic prediction schemes, and multicast routing protocols. These newer protocols designed for ATM networks will be able to guarantee certain quality of service which is important in many applications, particularly in the command and control area. Novel techniques based on neural networks were developed for admission control problem. Neural network techniques are quite suitable for such decision problems.

In traffic scheduling in input-buffered switches, it is possible to obtain high throughput with limited lookahead of the incoming traffic. There are many choices and our results were for the theoretical optimum case. For practical use, one can consider hardware implementation and modify our schemes slightly. The scheduling algorithm can also be used in IP switching in the Internet. The protocols for multicast routing developed in this project are scalable and can be used in large ATM networks.

The results obtained in this research were published in technical conferences and journals. Several papers are being prepared for submission to technical journals and conferences in the near future. This effort constituted significant portions of theses research of two PhD students and one MS student. The results from this research will have significant importance to the emerging ATM networks and for multimedia applications running on Gigabit networks.

8.1 Future Work

From our investigations on admission control and routing algorithms, we have identified several new research problems to work on. In admission control, when TCP/IP traffic with low data rates are mixed with video traffic we can expect the control algorithm to exhibit non-linear classification. It is interesting to study how our neural network will perform in such situations. Admission control algorithms need to be developed with different QoS requirements. In our studies, we used the average cell loss among all traffic as the QoS measure. We are working on an immediate extension to consider average delay as the QoS measure. Future work can be done with both cell loss and delay as QoS measures. Other extensions include cell loss and/or delay specified per connection, i.e., admit new connections only if QoS specified for each connection is not violated. We can also develop new algorithms based on measured data and the issue here is what traffic characteristics to measure and how to do this in a cost effective manner.

Input buffered ATM switches will become important for very high-speed networks as shared memory switch speeds are limited by memory bandwidth. We have just looked at one specific problem of scheduling traffic in an input buffered rearrangeably non-blocking (crossbar or Benes network) for achieving high throughput. Our throughput and delay results are obtained through simulations. Future work includes developing an analytical model to evaluate the throughput and delay, develop scheduling algorithm to be fair to all inputs by frame based scheduling, and consider hardware implementations of the algorithm. We are currently investigating simpler scheduling and routing algorithms suitable for Benes and Banyan networks, as the scheme based on bipartite matching is expensive. Another important work can be looking at scheduling multicast traffic in input-buffered switches. This is a very broad topic as some switches support multicast routing and the question is how to schedule multicasts without splitting and achieving high throughput. We can also investigate routing algorithms with QoS requirements.

The multicast routing algorithms developed in this project did not explicitly consider QoS requirements, but it is designed so that it can be modified to handle that. In the case of unicast traffic, the PNNI specification give the various QoS parameters. There is no such specification for multicasts to this date. For example, if we want bounded delay, does this mean that all receivers of a multicast must get the data within this time or only some, say majority of them. Just coming with a suitable QoS parameters for multicast traffic is itself a challenging topic. Assuming a QoS requirement is given, then the problems to research on include scalable multicast routing algorithms with QoS or what is known as QoS based routing, utilizing multicast ca-

pability of ATM switches to achieve network level QoS, and performance evaluations of such schemes. The QoS based routing is also of importance in the future Internet as many multimedia applications, e.g., video conference, distance learning etc., will demand such a service.

Another important problem related to multicast routing in ATM networks is the sender identification problem. We have begun some work on this problem which we call multiway communication. In a multicast group, it is possible that every receiver is also a sender. During a session, it is possible that many or all senders are sending data to the multicast group. Now, for better utilization of the resources, we would like to share the multicast tree for traffic from different senders. Then we need protocols to distinguish cells from different senders arriving at receivers. This is not an issue in the Internet as each packet has the sender information. However, in ATM networks with AAL5, only the header cell will contain such information. For better sharing of resources, it is useful to interleave cells from different while going through a common switch point. This means the switches must be able to route unambiguously such traffic for receivers to identify the senders. There are some solutions proposed to this problem at the ATM Forum and more investigations are needed to come up with a scalable solution to this sender identification problem in ATM networks.

9 List of Journal Publications

- R. Venkateswaran, C. S. Raghavendra, Xiaoqiang Chen, V. P. Kumar, "DMRP: A Distributed Multicast Routing Protocol for Dynamic Multicast Tree Computation," *IEEE/ACM Transactions on Networking* (submitted).
- Indu Mahadevan, C. S. Raghavendra, "ATM Admission Control at Node and Network Level Using Neural Networks," (in preparation for Journal on Selected Areas in Communication).

10 List of Conference Publications

- R. Drossu, T. V. Lakshman, Z. Obradovic, C. S. Raghavendra, "Single and Multiple Frame Video Traffic Prediction Using Neural Network Models," Proc. of the Networks'94 Conference, December 1994.
- RaSiRa95 Ram Krishnan, John A. Silvester, C. S. Raghavendra, "Jitter at an ATM Multiplexer in the Presence of Correlated Traffic" Proceedings IPCCC 95, March 1995.

- R. Venkateswaran, C. S. Raghavendra, "Multicast Switch Based on Tandem Expanded Delta Network" Proceedings Globecom 95, November 1995.
- Venkateswaran, R., Obradovic, Z., and Raghavendra, C.S. (1996) "Cooperative Genetic Algorithm for Optimization Problems in Distributed Computer Systems." *Proc. Second Online Workshop on Evolutionary Computation*, pp. 49-52, March 1996.
- R. Venkateswaran, C. S. Raghavendra, Xiaoqiang Chen, V. P. Kumar, "Hierarchical Multicast Routing in ATM Networks," Proceedings of ICC 96, June 1996.
- R. Venkateswaran, C. S. Raghavendra, Xiaoqiang Chen, V. P. Kumar, "Improved Algorithm for Multicast Routing in ATM Networks," Proceedings ICC 97, June 1997.
- Indu Mahadevan, C. S. Raghavendra, "Admission Control in ATM Networks using Fuzzy-ARTMAP," 1997 International Workshop on Applications of Neural Networks to Telecommunications, June 1997.
- C. S. Raghavendra, Rajneesh Kumar, Rajendra Boppana, "On ATM Cell Routing in Input-Buffered Switches," (in preparation for INFOCOM Conference)
- R. Venkateswaran, C. S. Raghavendra, "On Steiner tree in Unit Weight Internet like Networks," (in preparation for INFOCOM Conference).
- Indu Mahadevan, C. S. Raghavendra. "On Encapsulation of IP over ATM," (in preparation for a Networking Conference).
- Indu Mahadevan, C. S. Raghavendra, "QoS issues in multicast traffic routing over IP and ATM," (in preparation).
- H. Sivaraman, C. S. Raghavendra, "Performance of Communication Intensive Applications over ATM Networks" (in preparation).
- Rajendra Boppana, C. S. Raghavendra, "On ATM Cell Routing in Low Cost Input-Buffered Switches," (in preparation).

11 List of Personnel Associated with this Research Project

- Prof. C. S. Raghavendra, Principal Investigator for this Project

- R. Venkateswaran, PhD Student completing his degree in July 1997. Title of Dissertation – *Multicast Routing in High-Speed Networks*.
- Indu Mahadevan, PhD Student working on Admission Control and Resource Reservation.
- Rajneesh Kumar, MS Student graduated in May 1997. Title of Thesis – *On Cell Scheduling Algorithms for Input-Buffered ATM Switches*.

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